Claims

1. A processor operable to function in a multiprocessor computer system, the processor comprising:

a bus interface to provide communication with other processors;

a local cache;

a cache invalidation history table associated with the local cache; and

a cache controller associated with the local cache, the cache controller operable to track invalidated cache lines by recording the line addresses of invalidated cache lines and an indicator indicating whether each of the invalidated cache lines recorded was invalidated via a clean-invalidate or a dirty-invalidate in the invalidation history table, and further operable to revalidate only those invalidated cache lines recorded in the invalidation history table as having been clean-invalidate invalidated by monitoring the bus for cache line addresses of clean-invalidate invalidated cache lines recorded in the invalidation history table and for associated cache line data and by updating the invalidated cache line data with the cache line data associated with the recorded cache line addresses.

2. The processor of claim 1, further comprising a plurality of local caches local to the processor.

3. The processor of claim 1, wherein the processor is a part of a node, and further comprising at least one additional local cache local to the node.

4. The processor of claim 1, wherein the local cache is an L2 cache.

5. The processor of claim 1, wherein the local cache is a write-back cache.

6. The processor of claim 1, wherein the valid cache line data is present on

the bus due to a modified write-back.

7. The processor of claim 1, wherein the cache controller further comprises a write-back bit associated with entries in the local cache that is set when either a hit to the same line in another processor is detected or when the same line is invalidated in another processor's cache, and wherein the system broadcasts write-backs from a selected local cache only when the line being written back has an associated write-back bit set.

8. The processor of claim 7, wherein the selected local cache is an L1 cache.

9. The processor of claim 7, wherein the write-back bit is set only when the processor local to the local cache has write or exclusive write access to the line.

10. A cache control module associated with a local cache, the cache control module operable to track invalidated cache lines by recording the line addresses of invalidated cache lines and an indicator indicating whether each of the invalidated cache lines recorded was invalidated via a clean-invalidate or a dirty-invalidate in an invalidation history table, and further operable to revalidate only those invalidated cache lines recorded in the invalidation history table as having been clean-invalidate invalidated by monitoring the bus for cache line addresses of clean-invalidate invalidated cache lines recorded in the invalidation history table and for associated cache line data and by updating the invalidated cache line data with the cache line data associated with the recorded cache line addresses.

11. The cache control module of claim 10, wherein the cache control module comprises a part of an integrated circuit.

12. The cache control module of claim 11, wherein the integrated circuit

comprises part of a motherboard chipset.

13. The cache control module of claim 10, wherein the cache control module is embodied at least partially as software executable on a processor.

14. The cache control module of claim 10, wherein the valid cache line data is present on the bus due to a modified write-back.

15. The cache control module of claim 10, further comprising a write-back bit associated with entries in the local cache that is set when either a hit to the same line in another processor is detected or when the same line is invalidated in another processor's cache, and wherein the system broadcasts write-backs from a selected local cache only when the line being written back has an associated write-back bit set.

16. The cache control module of claim 15, wherein the selected local cache is an L1 cache.

17. The cache control module of claim 15, wherein the write-back bit is set only when the processor local to the local cache has write or exclusive write access to the line.